ALU and Sequential Logic Diagrams

CS207, Fall 2005
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1-bit ALU

32-bit ALU

S-R (set-reset) latch

- Unclocked memory device
- Basis for more complicated flip-flops and latches

<table>
<thead>
<tr>
<th>R</th>
<th>S</th>
<th>Q</th>
<th>Q'</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>previous value</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>unstable</td>
<td>unstable</td>
</tr>
</tbody>
</table>

D latch

- Stores the value of the input signal when the clock signal is “high”

D flip-flop

- Output is stored on the falling clock edge

D latches are in a “master-slave” configuration

Timing diagram
Q changes as clock signal moves from high to low

Finite state machine

• A sequential logic function that contains:
  – Set of states: all possible values that can be stored
  – Next-state function: maps current state and inputs to new state
  – Output function: maps current state and inputs to a set of (asserted) outputs