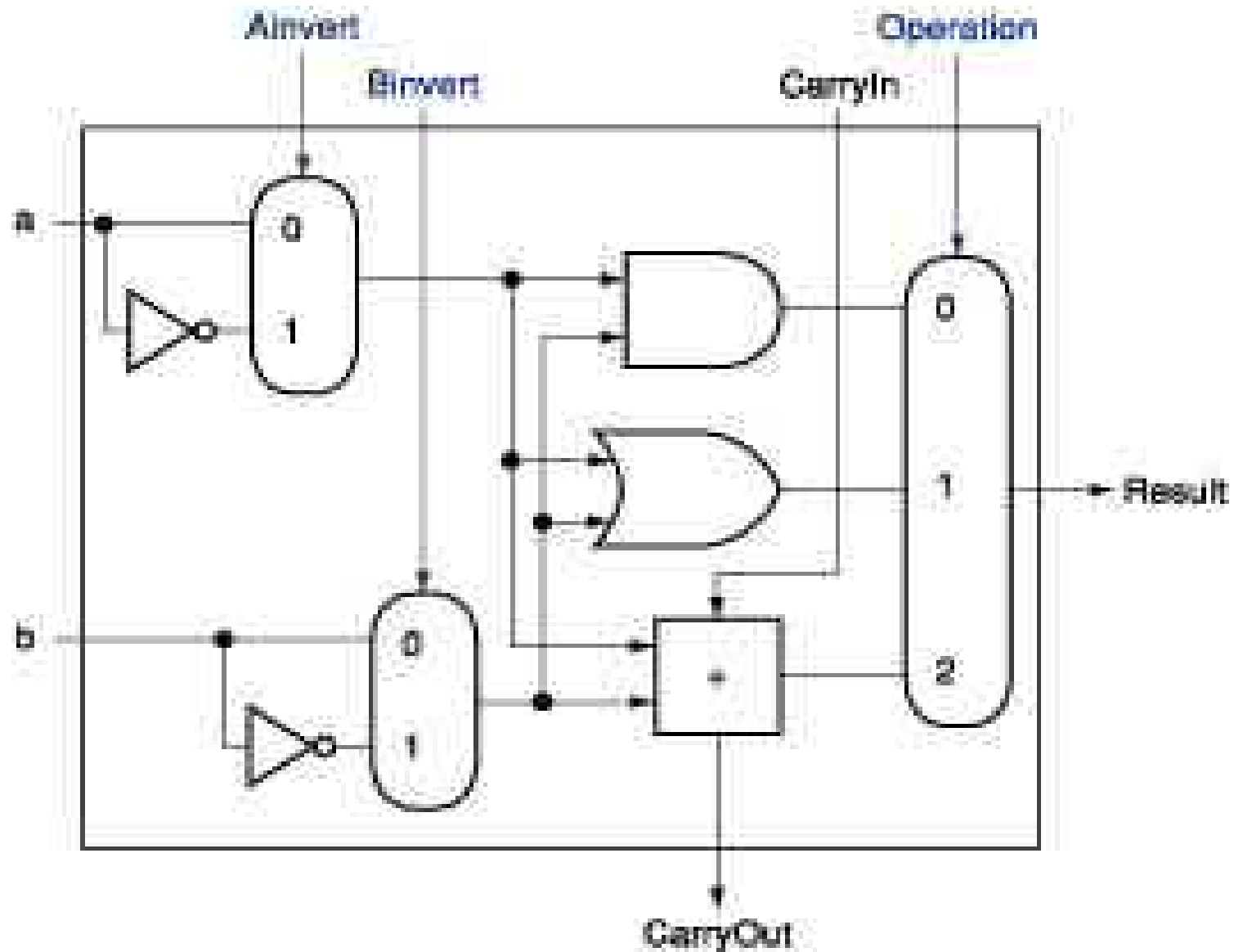


# ALU and Sequential Logic Diagrams

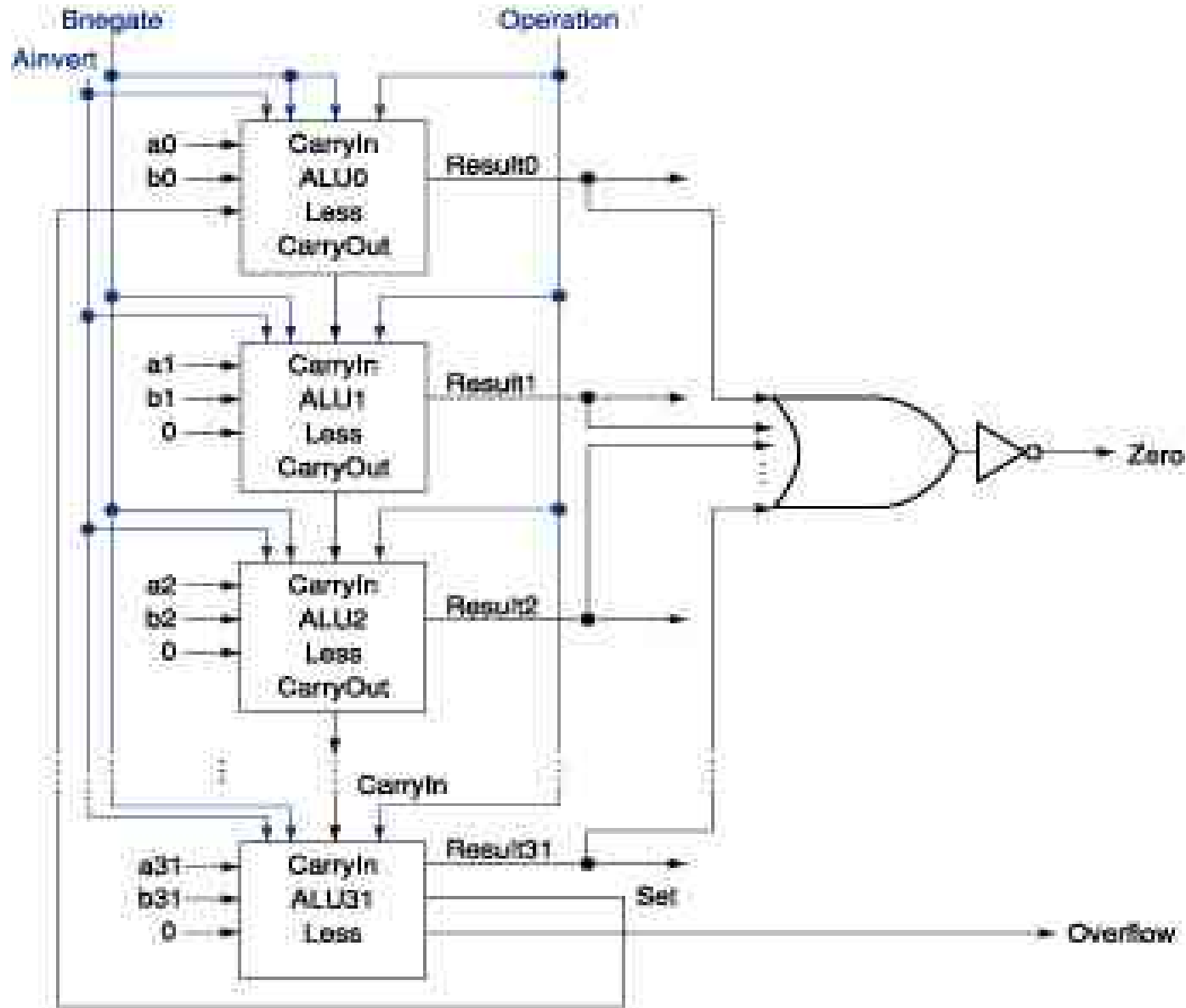
CS207, Fall 2005

October 14 and 19, 2005

# 1-bit ALU

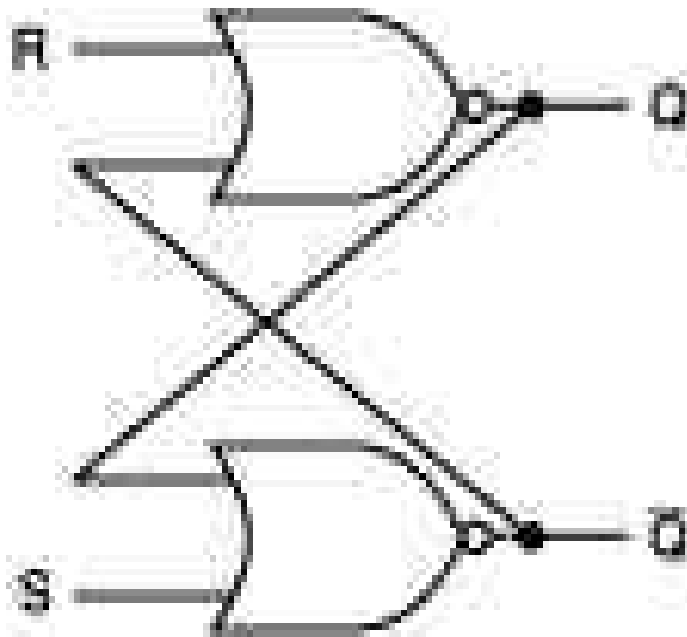


# 32-bit ALU



# S-R (set-reset) latch

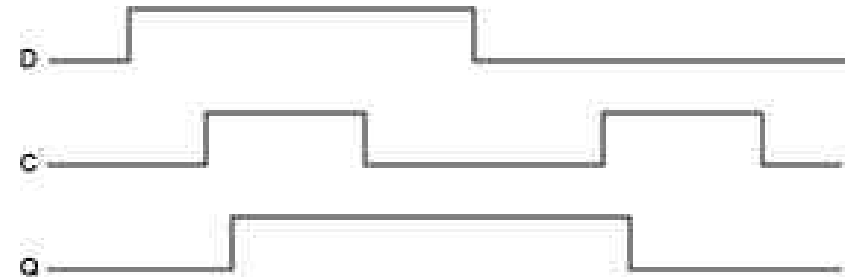
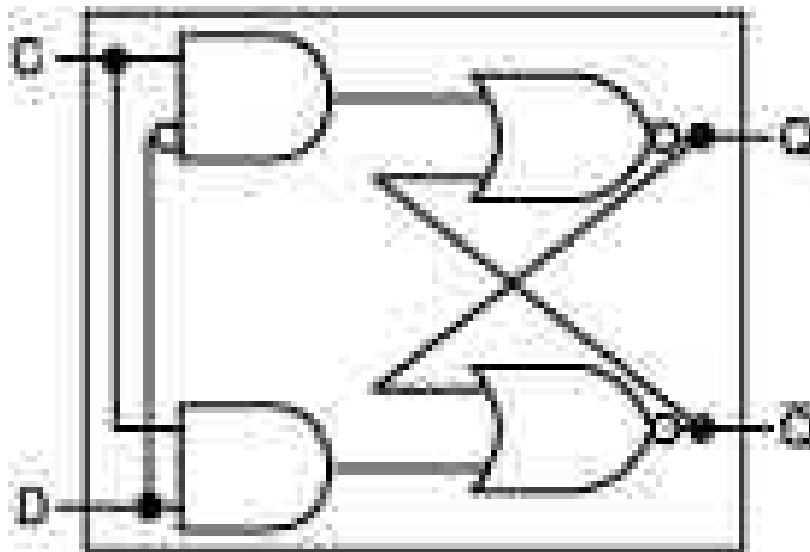
- Unclocked memory device
- Basis for more complicated flip-flops and latches



R	S	Q	Q'
0	0	previous value	previous value
0	1	1	0
1	0	0	1
1	1	unstable	unstable

# D latch

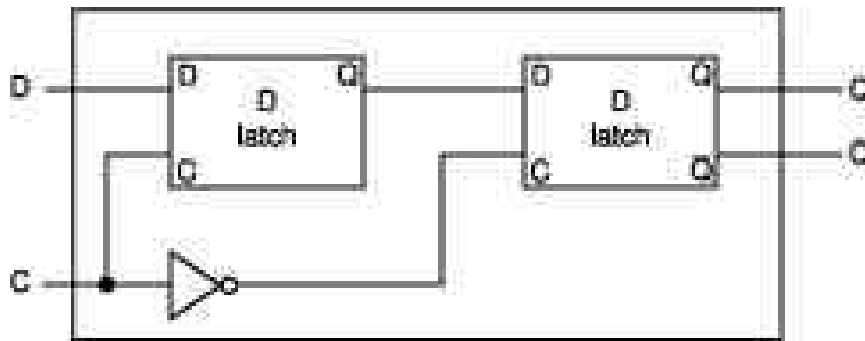
- Stores the value of the input signal when the clock signal is “high”



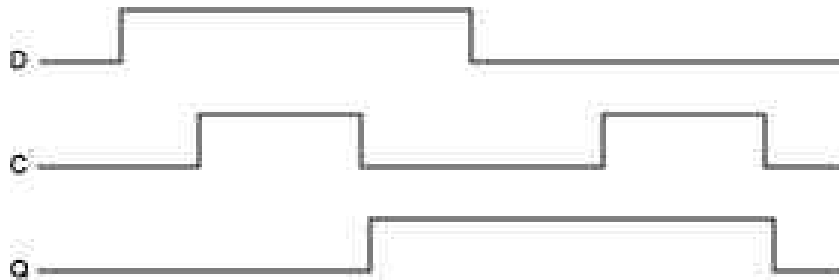
Timing diagram

# D flip-flop

- Output is stored on the falling clock edge



D latches are in a “master-slave” configuration



Timing diagram

Q changes as clock signal moves from high to low

# Finite state machine

- A sequential logic function that contains:
  - Set of states: all possible values that can be stored
  - Next-state function: maps current state and inputs to new state
  - Output function: maps current state and inputs to a set of (asserted) outputs

